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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/144,579	TSANG ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43,47-66,98-101 and 103* is/are pending in the application.

4a) Of the above claim(s) *98-101 and 103* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43 and 47-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

According to previous office actions, claims 43, 47-66, 98-101 and 103 are pending in this application; and claims 43 and 47-66 remain active in this office action.

Claim Objections

Claims 43 and 47-66 are objected to because of the following informalities:

Claim 43 recites the subject matters of "a gate conductor disposed over the gate oxide layer within the first trench to a depth of at least an elevation of the upper surface of the substrate", but fails to clarify which side (bottom or top) of the gate conductor reaches to the recited depth of at least an elevation of the upper surface of the substrate. It appears to be confusing, given that the upper surface (28') of the substrate in the instant invention (Figs. 9 and 10) is at a level between the bottom and top sides of the gate conductor (62).

Claims 43 recites the terms of "a first vertical layer portion" and " a body layer", but fails to clarify their relationship. And, according to the disclosure (see Figs. 11 and 12), the first vertical layer portion (90) is a portion of the body layer (26 or 26').

Claim 43 recites the terms of a "source contact" and "a second portion" of the recited upper metal layer", but fails to clarify their relationship. And, according to the disclosure (see Figs. 1 and 13), the two should be a same entity in the instant invention.

Claim 51 recites the term of "an insulative layer", but fails to clarify its relationship with the "an insulating layer" already defined in claim 43.

Appropriate correction is required.

Response to Amendment

The amendment filed on 12/14/2001 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The newly added three paragraphs starting with "Further to **such completion** and as incorporated herein by reference to U.S. Pat. No. 5,262,336, for example, a second layer of metal is deposited in gate pad regions of the gate contact layer in isolation from the source pads over a passivation layer" inserted on page 14, after line 28, appear to imply the subject matters that, further to the completion of the trench-gated type MOSFET shown in Fig. 12 in the instant invention, the contact structures (including source contact 28 and the gate contact 30) shown in Fig. 16B in US Patent 5,262,336 are further formed/applied to the structure shown in Fig. 12 in the instant invention. However, full support for such subject matters are not found in the original disclosure of the instant invention and/or in any of the original disclosures of its parent applications, including the ones of US Patents 4,895,810 and/or 5,262,336. None of these disclosures originally discloses that the contact structures including the ones shown in Fig. 16B in US Patent 5,262,336 and/or in Fig. 19 in US Patent 4,895,810 can

be used in the trench-gated type MOSFET of in the instant invention following the structure shown in Fig. 12 therein. In fact, the contact structures shown in the two patent patents are associated with planar-gate type MOSFET devices, which allows the simultaneous exposures of the source semiconductor region 24 and the gate conductor (32) during the depositing of the contact layer with two isolated portions (75 and 76 in Fig. 19 of 4,895,810; and/or, 28 and 30 in Fig. 16B of 5,262,336, wherein the contact 28 is not even in direct contact with the source region 24, instead the connection is via the doped region 67 in the base region 22). Obviously, such planar-type contact structures are not directly applicable to the trench-gated structure of the instant invention, given that the gate contact (62 in Fig. 12) in the active region is fully surrounded by insulating layers (60, 48 and 68) during the formation of the source contact (94).

And, applicant's relevant arguments filed on May 22, 2007 fail to adequately point out where in the previous patent applications and/or in the instant application it was taught/disclosed that the gate pad structure of a planar-gate type MOSFET device such as that taught in the previous patent applications can also be used in such a trench-gate type MOSFET as that in the instant application.

In fact, these newly added paragraphs which state that "a second layer of metal is deposited in gate pad regions of the gate contact layer in isolation from the source pads over a passivation layer" directly teach away from the original instant application, which specifically requires that the contact to the gate conductor to be done "without critical alignment, and passivating the surface" (see page 14, lines 25-28, in the original specification).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 43 and 47-66 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 43 recites the subject matters of "a first metal layer defining a gate metal layer overlying the doped polysilicon of the gate conductor; an insulating layer overlying the conductor; and an upper metal layer over the insulating layer and having a first portion contacting the gate conductor through a via in the insulating layer and a second portion coupled to the source region in electrical isolation from the gate conductor"

The subject matter recited in claim 43 about the "first metal layer" is found to be not fully supported by the original disclosures, since none of the above-mentioned disclosures originally discloses the subject matters a gate in the recited trench comprising the recited first metal in combination with the recited subject matter of the recited upper layer with the recited insulating layer therebetween.

Although the original instant application discloses that "a silicide layer can be formed in the remaining polysilicon layer" (see page 11, lines 27, through page 12, line 1), which does not necessarily mean in any way that a metal-only metal layer such as

that in the planar-gate of the relevant previous patent applications can also be formed in the instant application in a manner as that of the silicide layer. In the instant application, the gate is formed in the trench, which (see Figs. 6-8) naturally requires the step of etching back for the polysilicon layer in the trench. The silicide layer in the instant application can be readily formed through the method disclosed therein because the art-known self-aligned feature of the silicidation process, which allows the removing of the unreacted metal layer in a self-aligned manner for the remaining silicided layer. It is not clear how a metal-only layer such as the first metal layer recited in the claim could be patterned without having the self-aligned feature as that of the metal silicide layer.

And, applicant's relevant arguments filed on May 22, 2007 fail to adequately point out where in the previous patent applications and/or in the instant application it was taught/disclosed that the metal-only gate metal layer of a planar-gate type MOSFET device such as that taught in the previous patent applications can also be used as the recited first metal layer in the gate of the trench-gate type MOSFET as that in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43 and 47-66, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto (JP 3-109775; of record) in view of Cogan (US 5,164,325).

Sakamoto discloses a recessed gate field effect power MOS device (Figs. 1-7, especially 1, 4d, 5d, 6 and 7) having a vertically-oriented channel comprising:

a semiconductor substrate including first and second laterally-extending layers of first (p) and second (n) opposite polarity dopants defining a body layer (11; p type) and an underlying drain layer (3; n type);

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate insulating layer (7; which is commonly formed of an oxide layer in the art so as to have desired gate dielectric performance) on the trench sidewalls and the bottom wall of the first trench;

a gate conductor (8) disposed over the gate insulating layer within the first trench;

a vertically-oriented layer of semiconductor material extending upwardly along the gate oxide layer on the side thereof opposite the first trench, the vertically-oriented layer extending from the body layer to the upper surface of the substrate, the vertically-oriented layer comprising a first vertical layer portion (a portion of 11 that is in contact with the gate insulating layer 7) contiguous with the body layer and naturally defines an

active body region including a vertical channel, and a second vertical layer portion (12; n type) atop the first vertical layer portion and forming a PN junction therewith, the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region; and

a vertically-extending source conductor (15) contacting the vertically-oriented layer on a side thereof opposite the gate insulating layer and gate conductor, the source conductor electrically shorting the source region to the active body region across the PN junction;

the gate conductor comprising doped polysilicon (8) contacting the gate insulating layer within the trench; and

an insulating layer (9) overlying the gate conductor.

Although Sakamoto does not expressly disclose that the gate conductor in the embodiments of Figs. 1, 4d, 5d, 6 and 7 can further include a metal silicide layer, one of ordinary skill in the art would readily recognize that such a metal silicide layer can be desirably formed so as to increase the conductance of the gate conductor, as further evidenced in Sakamoto. In Fig. 2d of Sakamoto teaches to form a metal silicide (tungsten silicide) layer over the polysilicon layer in the gate conductor (8) in a MOSFET that is also a trench-gate type.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Sakamoto with a metal silicide layer being formed in the gate conductor, per the further teachings of Sakamoto, so that a MOSFET with increased conductance for the gate conductor therein would be obtained.

Furthermore, although Sakamoto does not expressly disclose that the device can further include upper metal layer, one of ordinary skill in the art would readily recognize that such a upper metal layer can be desirably formed so as to form the required source and gate contacts with reduced resistance, as readily evidenced in Cogan (see the upper metal layer including a first portion 116 and a second portion 111, a via in the insulating layer over the gate conductor 114, the source region 108).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make to incorporate the upper metal layer of Cogan into the device taught above by Sakamoto, so that a MOSFET with required source and gate contacts would be obtained.

Regarding claims 47 and 48, it is noted that the thicknesses of the semiconductor regions such as the ones as recited in the claims are art-recognized resulted-oriented parameters of importance subject to routine experimentation and optimization. And, it would be well within the ordinary skill in the art to form the device collectively taught above with the thicknesses for the vertical layer portions being substantially close to that as recited in the claims, so as to obtained a device with optimized performance, as it has been held that:

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 49 and 54, it is noted that it is well known in the art (as readily evidenced in Davies, US 4,960,723; of record; see Fig. 1) that the body region (21) can

be desirably doped heavier than that of the base region (17 and/or 20), so as to prevent parasitic bipolar transistor from being turned on.

Regarding claims 50-52, the device of Sakamoto further comprises the sidewall spacers (13).

Regarding claim 55, it is noted that it is well known in the art that the trench-gate type MOSFET device such as the one of Sakamoto can be desirably formed in a 2-D interconnected matrix, so as to increase the power and/or to decrease the on-resistance of the device.

Regarding claim 58, Sakamoto further discloses a p-type lower layer (1') in Fig. 7.

Regarding claim 59, Cogan further teaches the features of a first thickness (112a) thicker than the second thickness (112b), so as to improve the performance of the trench-gate type MOSFET.

Regarding claims 60-66, insofar as being in compliance with 35 U.S.C. 112, it is noted that each of the metals recited in the claims is an art-known metal material that is commonly recognized in the art to be used to form a metal silicide layer in a contact and/or electrode.

Response to Arguments

Applicant's arguments filed on May 22, 2007 have been fully considered but they are not fully persuasive. Responses to these arguments have been incorporated into the claim rejection and other relevant sections above.

Applicant's arguments regarding the art-rejections set forth in the 3-13-2003 office action have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment (filed on November 11, 2006) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
August 3, 2007

SHOUXIANG HU
PRIMARY EXAMINER